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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 1962-05416

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on December 8, 2006

Signature Ella R. Sisco

Typed or printed name Ella R. Sisco

Application Number	Filed
10/632,222	July 31, 2003

First Named Inventor: Gerard Chauvel

Art Unit	Examiner
2181	Jesse R. Moll

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☐ attorney or agent of record. Registration number _____
- ☑ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34: 57,365

Nick P. Patel
Signature

Nick P. Patel
Typed or printed name

(713) 238-8000
Telephone number

December 8, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Gerard CHAUVEL et al.	§	Confirmation No.	2081
Serial No.:	10/632,222	§	Group Art Unit:	2181
Filed:	July 31, 2003	§	Examiner:	Jesse R. MOLL
For:	Program Counter Adjustment Based On The Detection Of An Instruction Prefix	§	Atty. Docket No.:	1962-05416
		§	Client Ref. No.:	TI-35452

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: December 8, 2006

Sir:

Appellants hereby submit this Pre-Appeal Brief Request for Review in connection with the above-identified application. A Notice of Appeal is filed concurrently herewith.

I. Status of the Claims

In the *Final Office Action* dated September 6, 2006, all pending claims (claims 1-31) were finally rejected. Specifically, claims 1, 2, 7-12, 25 and 28-31 were rejected under 35 U.S.C. §103(a) as obvious under U.S. Patent No. 6,014,735 ("Chennupaty") in view of U.S. Patent No. 6,161,172 ("Narayan"). Claims 3, 4, 13, 15, 16 and 27 were rejected under 35 U.S.C. §103(a) as obvious under Chennupaty in view of Narayan and in further view of *New Bytecodes For "Real" Java?* (Google). Claims 5, 6, 14 and 26 were rejected under 35 U.S.C. §103(a) as being obvious under Chennupaty in view of Narayan and The JavaTM Virtual Machine Specification (JVM). Claims 17-20, 23 and 24 were rejected under 35 U.S.C. §103(a) as obvious under Chennupaty in view of Narayan and further in view of *Nazomi Introduces First Universal Java Accelerator Chip for Mobile Wireless Applications* (Nazomi). Claim 21 was rejected under 35 U.S.C. §103(a) as obvious under Chennupaty in view of Narayan, Nazomi and Google. Claim 22 was rejected under 35 U.S.C. §103(a) as obvious under Chennupaty in view of Narayan, Nazomi and JVM. Claims 1-31, a current listing of which is provided in the *Response and Amendment to Office Action Mailed January 4, 2006*, are hereby appealed.

II. Summary of Chennupaty

Chennupaty teaches a method and apparatus for encoding an instruction in an instruction set which uses a prefix code to qualify an existing opcode of an instruction. An opcode and an escape code are selected. The escape code is selected such that it is different from the prefix code and the existing opcode. The opcode, the escape code and the prefix code are combined to generate an instruction code which uniquely represents the operation performed by the instruction.

III. Claims

Claim 1 requires that "...the pre-decode logic determines whether a subsequent instruction comprises a prefix, in which case the decode logic causes a program counter to skip the prefix thereby precluding the decode logic from receiving the prefix..." The combination of Chennupaty and Narayan fails to teach or suggest precluding the decode logic from receiving the prefix by causing a program counter to skip the prefix.

Figure 4 of Chennupaty is reproduced below for convenience:

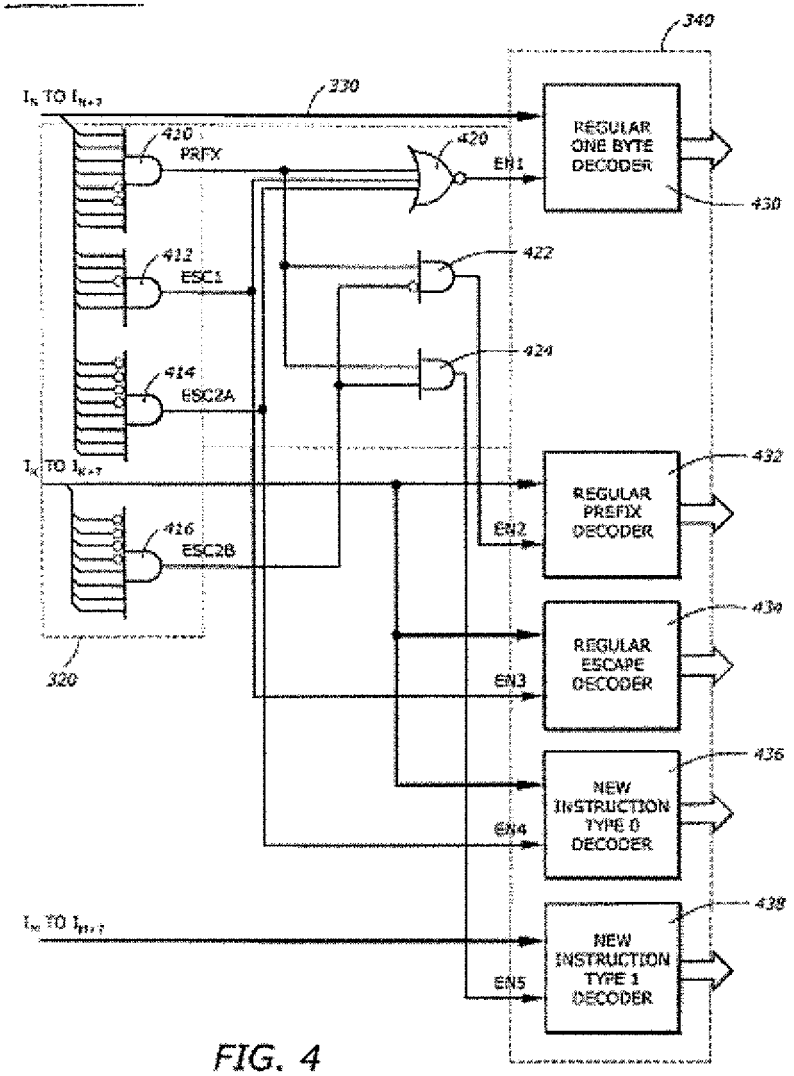


FIG. 4

Fig. 4 shows a decode unit containing a prefix and escape detector 320, a decoder enable circuit 330 and an opcode decoder 340. As described in col. 5, ll. 33-39, multiple bytes are provided to the decoder 340. Specifically, bytes I_N to I_{N+7}, I_K to I_{K+7} and I_M to I_{M+7} are provided to the decoder 340. In many cases, the byte I_N to I_{N+7} is a prefix. If the byte I_N to I_{N+7} is a prefix, col. 5, ll. 59-65 state that the output enable signal EN1 of NOR gate 420 is negated. Because the enable signal EN1 is negated, the decoder 430 is disabled, thereby precluding the decoder 430 (and the decoder 340 in general) from receiving the byte I_N to I_{N+7} (that is, the prefix).

Although the prefix is precluded from being received by the decoder 340, Appellants point out that the technique ***by which*** the prefix is kept out of the decoder 340 is different than

what is required by claim 1. Claim 1 requires that the decode logic is precluded "from receiving the prefix" because "the decode logic causes a program counter to skip the prefix." That is not the case with Chennupaty. In Chennupaty, hardware logic (*i.e.*, the gates 410, 412, 414 and 420) prevents the decoder 340 from receiving the prefix. It is not the adjustment of a program counter that causes the prefix to be rejected by the decoder 340, as required by claim 1; instead, it is hardware logic that is responsible for preventing the decoder 340 from receiving the prefix.

Appellants notice that the Examiner asserts, "Further note that if the first byte is a valid prefix, the first byte is ignored by the decoder ... in effect causing the program counter (pointer to the current instruction) to skip the prefix bytes and point to the instruction being decoded" (p. 3 of the Office Action dated September 6, 2006). Appellants provide two comments in response. First, Chennupaty's program counter setup is not explicitly disclosed. The program counter may very well point to the next instruction to be fetched, and if this is the case, then the program counter would not be altered by the decoder 340's rejection of the prefix (since the prefix has already been issued from the instruction buffer 310). Second, what happens to Chennupaty's program counter as a result of the decoder 340's rejection of the prefix is irrelevant. Claim 1 states that the "program counter [skips] the prefix," thereby ***causing*** the decoder to reject the prefix. In Chennupaty, the cause-effect relationship is reversed from what is required by claim 1: adjustment of the program counter, if it happens at all, would be an ***effect*** of the decoder 340's rejection of the prefix. Narayan, Google, JVM and Nazomi all fail to satisfy the deficiencies of Chennupaty.

In summary, all combinations of the cited references fail to teach precluding a prefix from being received by a decoder by causing a program counter to skip the prefix. Specifically, Chennupaty discloses that the decoder 340 is prevented from receiving the prefix due to the hardware gates 410, 412, 414 and 420 (***not*** due to the adjustment of a program counter), and Narayan, Google, JVM and Nazomi all fail to satisfy the deficiencies of Chennupaty.

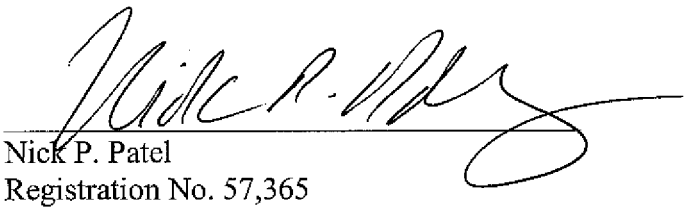
Based on any or all of the foregoing, claim 1 is patentable over all combinations of the art of record. Because claim 1 is patentable, its dependent claims 2-8 also are patentable. Further, because independent claims 9, 17 and 25 comprise limitations similar to those of claim 1, claims 9, 17 and 25 and their dependent claims 10-16, 18-24 and 26-31 also are patentable over all combinations of the art of record.

IV. Conclusion

In the course of the foregoing discussions, Appellants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Appellants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.36(a), and any fees required are hereby charged to Texas Instruments Inc.'s Deposit Account No. 20-0668.

Respectfully submitted,



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